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System-Level Integrated Circuit (SLIC) Development For Phased Array Antenna Applications

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System-Level Integrated Circuit (SLIC) Development For Phased Array Antenna Applications

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ABSTRACT

This paper describes a microwave/millimeter-wave system-level integrated circuit (SLIC) being developed for use in phased array antenna applications. The program goal is to design, fabricate, test, and deliver an advanced integrated circuit that merges radio-frequency (RF) monolithic microwave integrated circuit (MMIC) technologies with digital, photonic, and analog circuitry that provide control, support, and interface functions. As a whole, the SLIC will offer improvements in RF device performance, uniformity, and stability while enabling accurate, rapid, repeatable control of the RF signal. Furthermore, the SLIC program addresses issues relating to insertion of solid state devices into antenna systems, such as the reduction in number of bias, control, and signal lines. Program goals, approach, and status will be discussed.

1. INTRODUCTION

Electronically steered phased arrays provide the capability for scanning, tracking, beam shaping, adaptive nulling, and other important antenna functions. The use of monolithic microwave integrated circuit (MMIC) phase shifters, variable power amplifiers, low noise amplifiers, etc in arrays offers the potential for increased array functional capability at lower weight, smaller size, and ultimately, lower cost than conventional approaches based on discrete devices. Government and industry have been highly successful in developing and demonstrating MMICs at frequencies to K_a-band and higher. Large investments in circuit design and material and fabrication technology development have succeeded in extending individual circuit performance levels in terms of device characteristics such as frequency, efficiency, bandwidth, noise figure, etc. NASA Lewis Research Center has invested a significant portion of its space electronics R&D resources to sponsor a number of successful industry efforts to develop K-band, K_a-band and higher frequency MMICs appropriate for space communication subsystems including antennas, amplifiers, and receivers.

The demonstration in the laboratory of a single (or few) "circuit level" devices is an essential first step in the long journey to achieving a functional array of N radiating elements involving many MMIC devices (e.g. N phase shifters, N amplifiers) working reliably, predictably, and stably together in a space environment. What are required are "system-level" integrated circuits (SLICs) that build upon the existing circuit level technology and specifically address the issues associated with MMIC insertion into the complex array system environment. The following sections identify insertion issues and outline a proposed program for SLIC development.

2. BACKGROUND

The central problem in MMIC array development is the integration of large numbers of MMIC devices in a very compact space envelope. Figure 1 shows a conceptual drawing of a MMIC-based phased array used as a feed in a reflector system. Typical placement of the radiating elements, MMIC devices, and beam forming network are shown. The design shown illustrates a transmit-only configuration, in which RF and control signals originate at a central controller that is spatially remote from the antenna radiation plane. The RF signal is routed by the beam forming network to MMICs that are positioned directly behind independent microstrip patch radiators. The placement of the MMICs

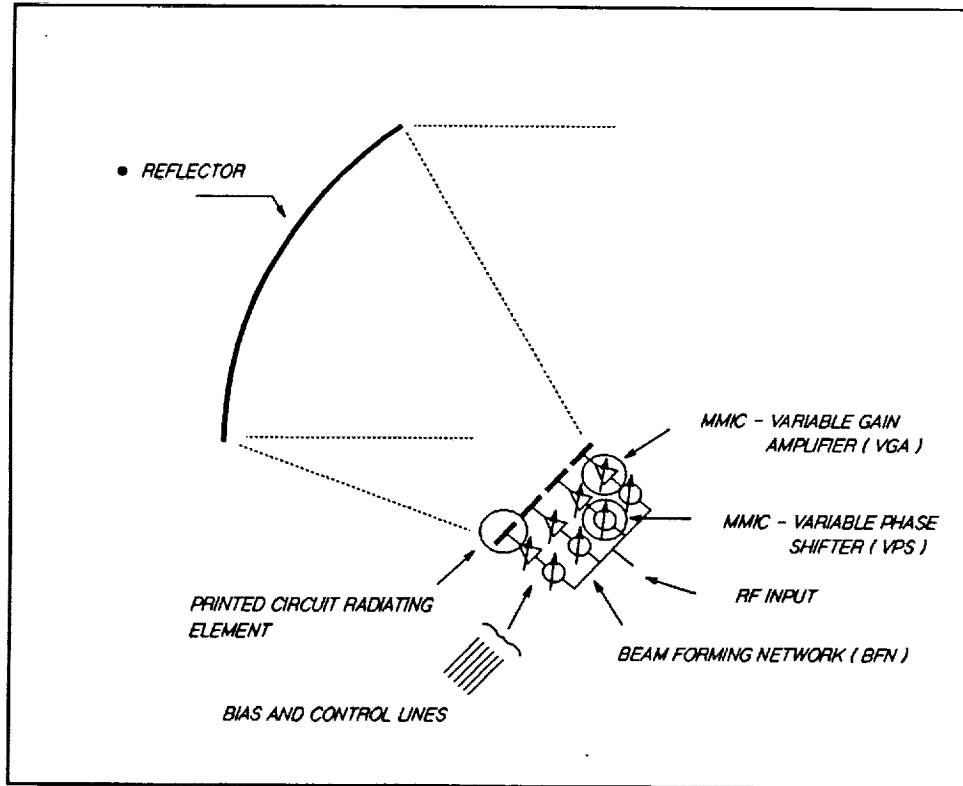


Figure 1: MMIC phased array feed with reflector

behind the radiators provides individual control of each element's amplitude and phase characteristic, but is greatly restrained by lack of available space behind the radiating element. Based on grating lobe considerations, the center-to-center spacing of the radiating elements is optimum near one half of a wavelength. For K_a -band, this limits the physical useable area to approximately 0.5 cm squared, which typically approaches the physical dimensions of the MMIC itself. The MMIC package, if used, is also required to fit within this space, along with RF, bias, and control line connections.

A look at some existing MMICs illustrates another aspect of the device integration problem. The devices chosen have representative MMIC interface, bias, control and physical layout characteristics. (RF characteristics are not discussed, and no endorsement of design or manufacturer is intended.)

Figure 2 displays a 30 GHz MMIC phase shifter¹. The chip consists of 4 independent phase shift bits (180, 90, 45, and 22.5 degrees) providing a minimum of 16 randomly selectable phase shift states. The 180°, 90°, and 45° bits are switched line type, operated by applying complementary biases to pairs of switching FETs. This action switches in and out precise lengths of microstrip line, thus providing a true time delay phase shift. The fourth and least significant bit is a loaded line type that is designed to deliver a continuously variable electrical delay over the range of 0 to 22.5 degrees. This device illustrates typical K_a-band phase shifter MMIC characteristics in terms of bias (control) line requirements and chip size (0.10" x 0.25"). In this case, a minimum of seven (7) lines are required to operate the phase shifter, in addition to the microstrip input and output lines. The control lines for the switched line bits are dual state and generally compatible with TTL logic.

Figure 3 displays a 20 GHz receiver circuit including both an amplifier section and a three-bit phase shifter on a single substrate². The phase shifter is a switched-line type, operated by complementary biases on control pads. Both the low-noise amplifier stage and a buffer stage are independently controllable. Due to the large functional capability, the chip requires 12 bias connections for full operation, plus the RF input and output microstrip. In addition to the high level of integration, a design feature of the circuit is the placement of all bias connections along one side of the chip, facilitating testing and system layout.

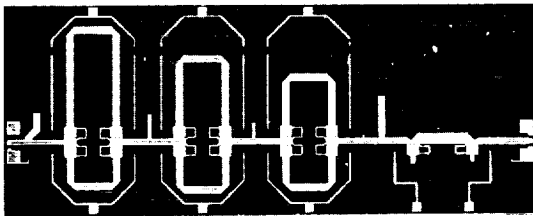


Figure 2: Honeywell phase shifter



Figure 3: Rockwell receiver chip

Figure 4 displays a MMIC variable gain amplifier chip³. The chip features four stages of amplification and operates at 20 GHz. Variable gain is provided by a second gate in each FET, controlled through an on-chip, 4-bit, digital-to-analog convertor. This chip requires ten bias lines for operation but demonstrates the integration of a control circuit on the RF substrate.

A common characteristic of these representative MMICs is the number of control and bias lines required. This is not a serious problem when testing or demonstrating a single MMIC in a laboratory environment. However, the line count becomes a significant issue when large numbers of MMICs are assembled into arrays. The three MMIC devices described above illustrate the need to reduce the number of bias and control input lines by incorporating circuits for

¹: NASA Contract NAS3-23356, Honeywell Sensors and Signal Processing Laboratory.

²: USAF Rome Labs, Contract F19628-83-C-0108, Rockwell International

³: NASA Contract NAS3-22886, Texas Instruments Central Research Laboratory

power conditioning and control demultiplexing. In general, the devices described operate at voltages compatible with established TTL logic families, allowing control circuits to be merged with RF functions. Switching speeds are also well below demonstrated digital capabilities. In some cases, physical space is already available on the microwave substrate to locate at least some portion of the interface and control circuitry. Power conditioning features are already beginning to be added to some MMIC devices.

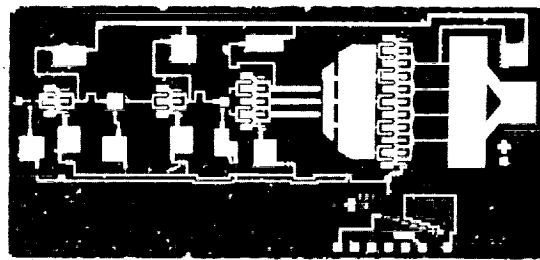


Figure 4: TI Variable power amplifier

3. PROGRAM GOALS

The goal of the SLIC development program is to take a microwave/millimeter wave RF MMIC phase shifter circuit and add to it (or incorporate into it) ancillary circuits providing functions such as power conditioning, bias control and regulation, device protection, thermal compensation, control processing, optical interfacing, and device health and status monitoring that will reduce the interconnect requirements of each MMIC and will regulate and control each device to provide reliable, repeatable, optimized performance. It must be emphasized that the thrust of the SLIC development effort is to be directed toward adding these features to existing MMICs and not toward developing improved MMIC devices. ("Circuit level" MMIC device enhancements will of course continue to be the focus of much of the industry activities and will be ultimately find their way into SLICs.)

A conceptual drawing summarizing potential features of a SLIC is presented in Figure 5. The figure illustrates some of the overall features and functions that are of interest in the SLIC integration efforts. The selection of circuits is intended only to illustrate the SLIC concept, and the layout shown is arbitrary.

The first function of interest in the SLIC is that of power conditioning. The main goal of this circuit is to include a means by which voltage division, voltage regulation, static protection, and overvoltage protection is directly incorporated with the RF MMIC as needed. This function becomes most desirable when working with amplifiers, where multiple biases are required to operate the devices at repeatable, known conditions. Additionally, this function is important for high sensitivity circuits where protection circuitry is needed to avoid damage to the devices. From a system standpoint, the on-chip power conditioning function also has the capability to substantially reduce the number of bias lines required for each RF MMIC, by converting a common "rail" voltage to those biases needed for that specific RF MMIC. Provisions could be made so that non-uniformities in bias levels from chip-to-chip could be compensated using quasi-variable power conditioning circuits.

For amplifier and analog phase shifter circuits, on-board bias control and temperature compensation circuits offer possible advantages over conventional MMICs. Together with sensing circuitry, it is envisioned that automatic correction can be applied to the bias of the MMIC to correct for temperature drift. This is especially important in a large array configuration, where it is likely that the various RF circuits may experience different thermal environments depending on location within the array structure.

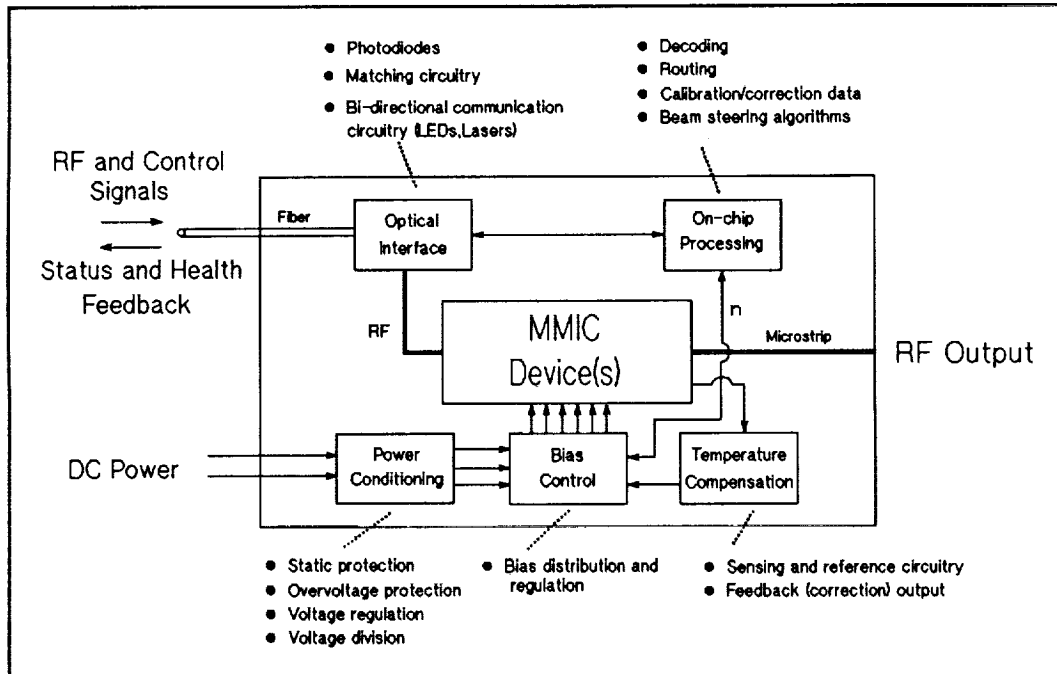


Figure 5: System-Level Integrated Circuit (SLIC) Concept

For variable power amplifiers and especially for multi-bit phase shifters, the on-chip processing circuits offer the possibility of major reduction in control line count and improvements in functional capability. Using a serial data stream input, the circuit could potentially offer full control of the RF MMIC, implementing beam steering algorithms (as appropriate) and applying correction or calibration data to the device control signals. Memory registers could be pre-programmed to contain calibration data or address information as needed. Due to the level of maturity of digital circuitry, this particular circuit offers the greatest flexibility within the SLIC and provides fertile ground for creative design.

The optical interface portion of the SLIC block diagram is perhaps the most challenging aspect of the development program, but at the same time offers the opportunity for some of the most significant advances in MMIC array technology. Microstrip transmission lines, typically used in applications at K_a -band frequencies to route RF and control signals, have well known capabilities and performance, but are less desirable due to insertion losses and mechanical inflexibility. Recent research efforts in the optics field have demonstrated the suitability of fiber optics as a replacement for microstrip to be used as both the RF and control signal interfaces for SLIC devices. The obvious mechanical and electrical advantages of the fiber optic components suggest that their integration into phased array antenna systems would provide improved performance and capability. For this reason, the integration of optical (photonic) circuitry into the SLIC design is desirable. Figure 5 shows both RF and control signals multiplexed on a single optical fiber interface. Less aggressive but still attractive approaches might bring only the MMIC control information in via a fiber optic interface or bring the control and RF signals in on separate optical fibers.

In general the goal of the SLIC program is to develop an advanced circuit incorporating an existing phase shifter MMIC design with control, support, and interface functions providing stable, uniform operation in an array environment. The circuit should minimize the number of signal, control and bias lines through appropriate use of fiber optics, multiplexing,

on-chip processing and on-chip dc power distribution. The overall design should take into consideration array size, architecture, radiating element spacing, and function. The list of program objectives for the system level integrated circuit may appear ambitious in scope, but it does reflect the desired level of integration and function required in many phased array applications.

4. APPROACH

In order to support the insertion of MMIC technology into arrays for NASA and commercial missions, the NASA Lewis Research Center (LeRC) is planning a SLIC development contract. The contract scope will encompass the design, fabrication, test and delivery of a number of SLIC devices addressing the issues described above. The authors believe that this program will encourage and enable the industry to take this important, system-oriented, MMIC insertion step, drawing on many circuit design and fabrication technologies already receiving considerable attention.

The emphasis of the contractual effort is directed toward integration of support, control, and interface circuits with established MMIC technologies. It is intended that an existing RF MMIC circuit (phase shifter) be used as a baseline to which additional circuits are added or incorporated to realize as many of the SLIC contract goals as possible. The thrust of the initial work will be on determining the optimum combination and level of integration of the various analog, digital and/or optical circuits. Since a variety of processing technologies may be involved, it is recognized that some processing research and development may be necessary. While a fully monolithic SLIC (an MSLIC, with all circuits on a single substrate) is desirable, it is understood that a hybrid implementation may represent the most reasonable approach in this initial SLIC contract.

The support and interface circuits to be utilized in the SLIC designs are to be developed in a generic sense, optimizing performance for a moderate range of MMIC devices and possible applications. It is intended that some of the SLICs be packaged, permitting their integration and demonstration in subarrays in post contract LeRC in-house investigations.

5. SUMMARY

It has been proposed that the development of the system-level integrated circuits (SLICs), building upon existing high performance RF MMIC devices, will greatly facilitate the integration of these devices in advanced phased array antenna systems. A concept for the SLIC has been presented to indicate some of the many possible features and capabilities and to stimulate discussion. The SLIC approach will ease the operating requirements and complexity of the antenna power supply and controller subsystems, and provide optimized and controlled RF MMIC performance. Additionally, the SLIC will offer size, weight, and mechanical flexibility advantages that should substantially cut costs and expedite application of MMICs in NASA and commercial missions.

The appeal of the SLIC approach to array designers is that by bringing more system functional capability down to the device level, the requirements for external device supporting control and power systems and their attendant interconnects can be reduced and device performance, stability and uniformity increased. The resulting impact on array functional capability, performance, size, and cost can be very significant.



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